University of Siena

TERA^{F}LUX.EU

Barcelona
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Exploiting Dataflow Parallelism in Teradevice Computing

University of Augsburg

a Proposal to

Harness the Future Multicores

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Edinburgh – HiPEAC Computing Week

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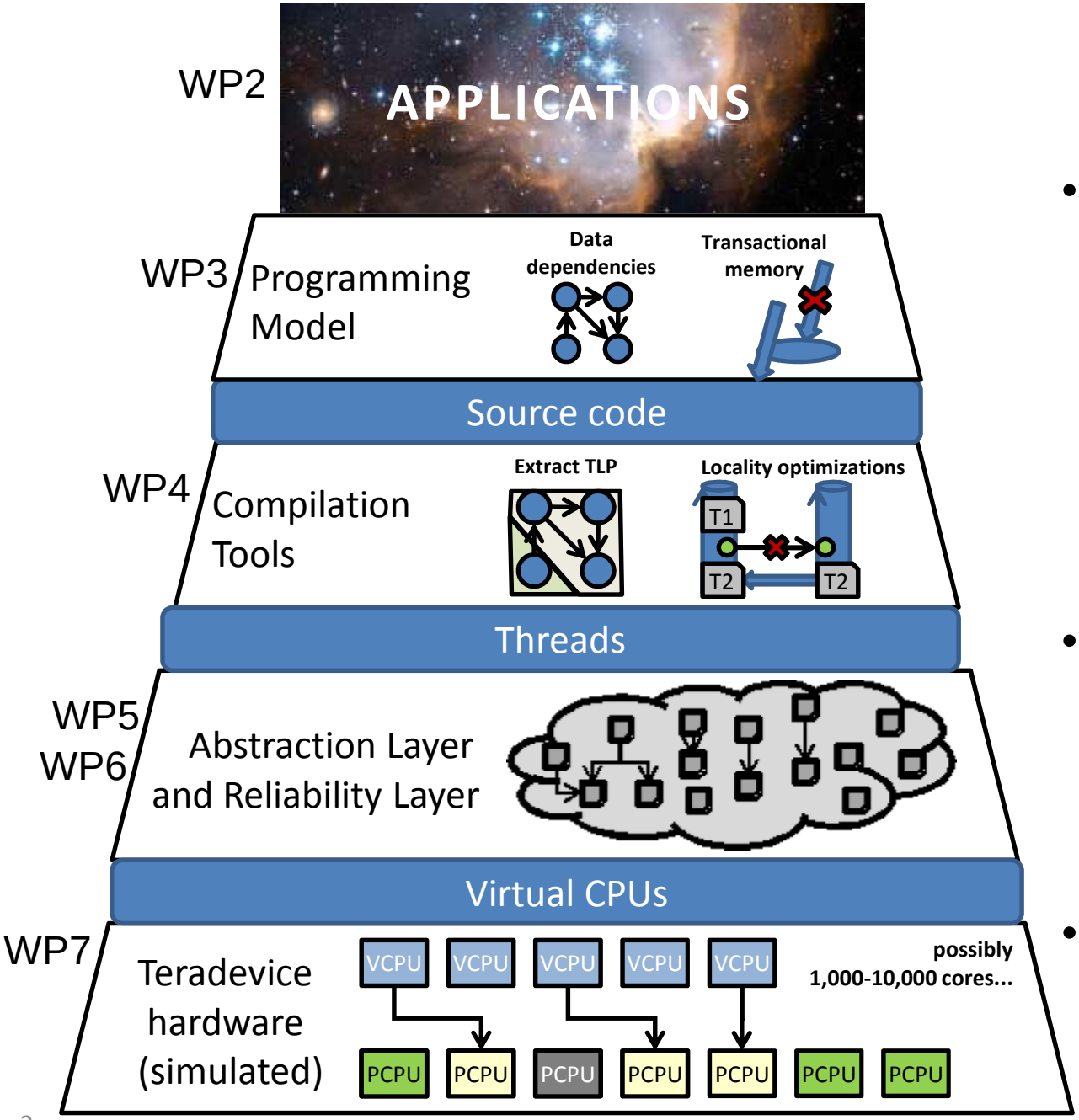

TERAFLUX

What is about

- 1000 Billion- or 1 TERA-device computing platforms pose new challenges:
  - (at least) programmability, complexity of design, reliability
- TERAFLUX context:
  - High performance computing and applications (not necessarily embedded)
- TERAFLUX scope:
  - Exploiting a less exploited path (DATAFLOW) at each level of abstraction

TERAFLUX key results we are aiming at & long term impact

- Coarse grain dataflow model (or fine grain multithreaded model)
  - fine grain transactional isolation
  - scalable to many cores and distributed memory
  - with built-in application-unaware resilience
  - with novel hardware support structures as needed
- A solid and open evaluation platform based on an x86 simulator based on COTSon by TERAFLUX partner HPLabs (http://cotson.sourceforge.net/)
  - enables leveraging the large software body out there (OS, middleware, libraries, applications)

TERAFLUX: toward a different world

- Relying on existing architectures as much as possible and introduce key modifications to enhance programmability, simplicity of design, reliability.
  - not a brand new language, but leverage and extend other open efforts [C+TM, SCALA, OPEN-MP]
  - not a brand new system, but leverage and extend other open software frameworks [GCC]
  - not a brand new CPU architecture, but leverage and extend industry standard commodities [x86]
- However: the implications on “classical limitations” can be huge
  - requirements of the hardware memory architecture which limit extensibility (a.k.a. scalability) can be relaxed significantly
  - Turning dataflow model into a general purpose approach through the addition of transactions

Technical problems to be addressed in Computing Systems

- Teradevices: new challenges are posed by the huge number of transistors and cores available on a chip. Once again:
  - Programmability
  - Effective Architectures
  - Reliability and Real-time

THANKS FOR YOUR ATTENTION