# Prof. Israel Koren

## Defect Reduction and Fault Tolerance in VLSI Integrated Circuits

**Aula 145 – 27 Maggio 2010 ore 12**

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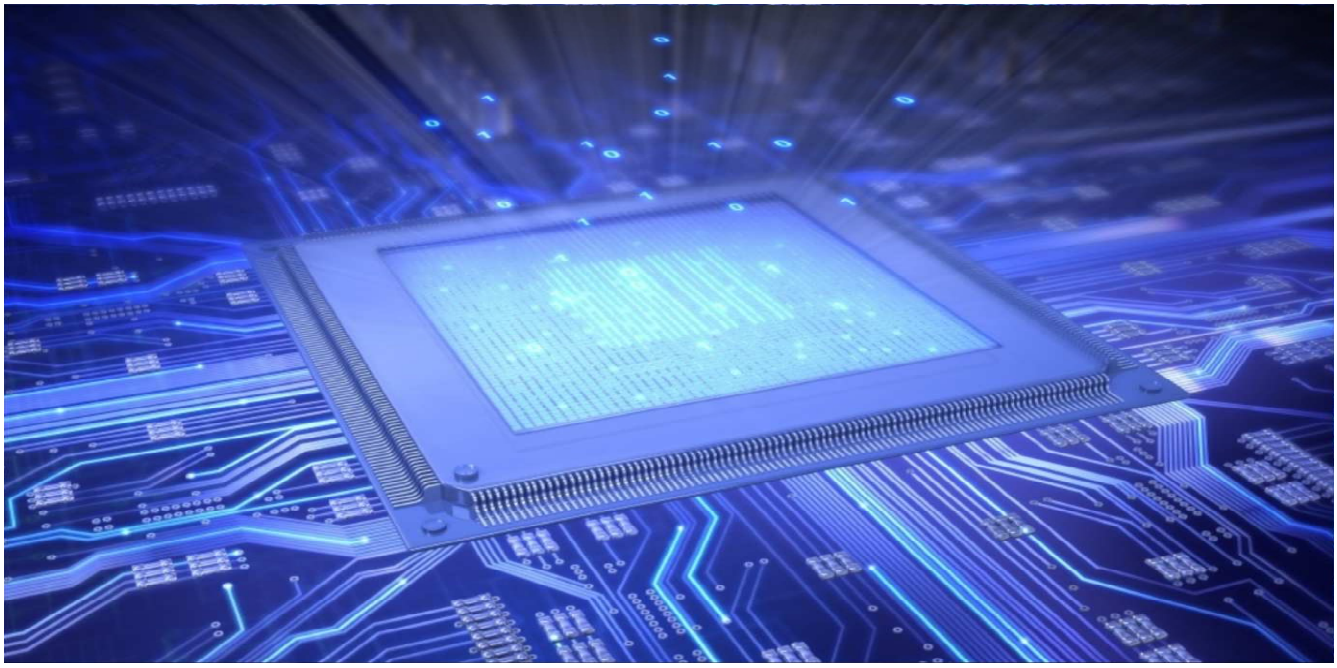


Abstract:

Advances in VLSI technology allow now the integration of hundreds of millions of devices in a single IC (e.g., a quad-core microprocessor) at an increasing device density. This trend unfortunately, also increases the likelihood of manufacturing defects, which if ignored, will result in a very low yield, where yield is the percentage of good ICs out of a manufactured wafer. Techniques to reduce the number of defects and tolerate the few that may still occur have been developed and are increasingly being used in the design of recent VLSI ICs, in general, and microprocessors, in particular. In this talk we first describe the types of defects that modern VLSI ICs are experiencing. We then briefly discuss the approaches used to identify the areas of the chip that are most sensitive to manufacturing defects and present the way yields of future ICs are predicted. Finally, we describe the currently employed techniques for reducing the number of chip-kill defects and for tolerating the defects that still remain.


Bio:

Israel Koren is a Professor of Electrical and Computer Engineering at the University of Massachusetts, Amherst and a fellow of the IEEE. He has been a consultant to companies like IBM, Analog Devices, Intel, AMD and National Semiconductors. His research interests include Fault-Tolerant systems, secure cryptographic devices, VLSI yield and reliability and Computer Arithmetic. He publishes extensively and has over 200 publications in refereed journals and conferences. He is the author of the textbook "Computer Arithmetic Algorithms," 2nd Edition, A.K. Peters, Ltd., 2002, a co-author of the textbook "Fault Tolerant Systems," Morgan-Kaufman, 2007.

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